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FAIRCHILD SEMICONDUCTOR TM

December 2000

QFET™

FQPF1P50

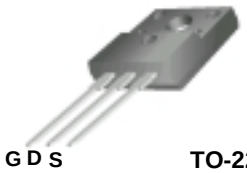
500V P-Channel MOSFET

General Description

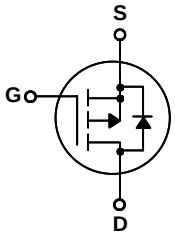
These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand a high energy pulse in the avalanche and commutation modes. These devices are well suited for electronic lamp ballasts based on the complementary half bridge topology.

Features

- -1.03A, -500V, $R_{DS(on)}$ = 10.5Ω @V_{GS} = -10 V
- Low gate charge (typical 11 nC)
- Low Crss (typical 6.0 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



TO-220F
FQPF Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		FQPF1P50	Units
V_{DSS}	Drain-Source Voltage		-500	V
I_D	Drain Current - Continuous (T_C = 25°C)		-1.03	A
	- Continuous (T_C = 100°C)		-0.65	A
I_{DM}	Drain Current - Pulsed	(Note 1)	-4.12	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	110	mJ
I_{AR}	Avalanche Current	(Note 1)	-1.03	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	2.8	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	-4.5	V/ns
P_D	Power Dissipation (T_C = 25°C)		28	W
	- Derate above 25°C		0.22	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	4.46	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

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Elerical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 μA	-400	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25°C	--	-	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -500 V, V_{GS} = 0 V	--	--	-1	μA
		V_{DS} = -400 V, T_C = 125°C	--	--	-10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 μA	-3.0	--	-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -0.515 A	--	8.0	10.5	Ω
g_{FS}	Forward Transconductance	V_{DS} = -50 V, I_D = -0.515 A (Note 4)	--	1.03	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz	--	270	350	pF
C_{oss}	Output Capacitance		--	40	50	pF
C_{rss}	Reverse Transfer Capacitance		--	6.0	8.0	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -250 V, I_D = -1.5 A, R_G = 25 Ω (Note 4, 5)	--	9.0	30	ns
t_r	Turn-On Rise Time		--	25	60	ns
$t_{d(off)}$	Turn-Off Delay Time		--	27	65	ns
t_f	Turn-Off Fall Time		--	30	70	ns
Q_g	Total Gate Charge	V_{DS} = -400 V, I_D = -1.5 A, V_{GS} = -10 V (Note 4, 5)	--	11	14	nC
Q_{gs}	Gate-Source Charge		--	2.0	--	nC
Q_{gd}	Gate-Drain Charge		--	5.6	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	-1.03	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-4.12	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.03 A	--	--	-5.0	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = -1.5 A, dI_F / dt = 100 A/μs (Note 4)	--	200	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.7	--	μC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 187mH, I_{AS} = -1.03A, V_{DD} = -50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ -1.5A, di/dt ≤ 200A/μs, V_{DD} ≤ $BV_{DSS,}$ Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

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Typical Characteristics

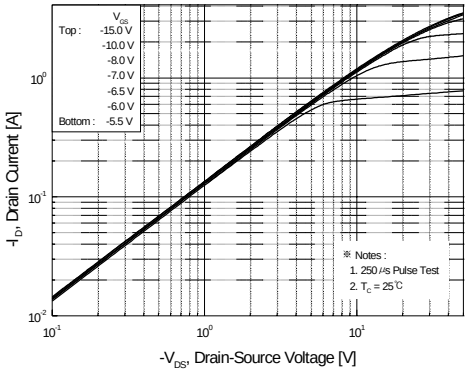

Figure 1. On-Region Characteristics

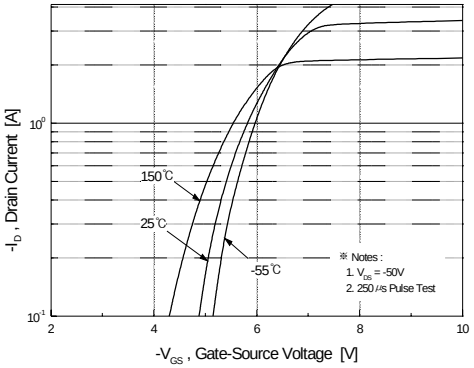

Figure 2. Transfer Characteristics

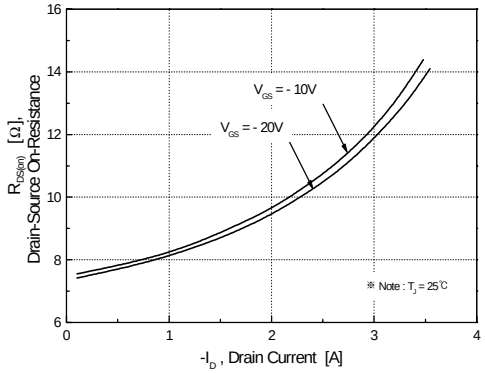

Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

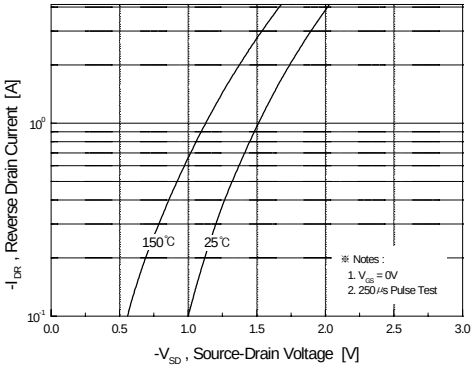

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

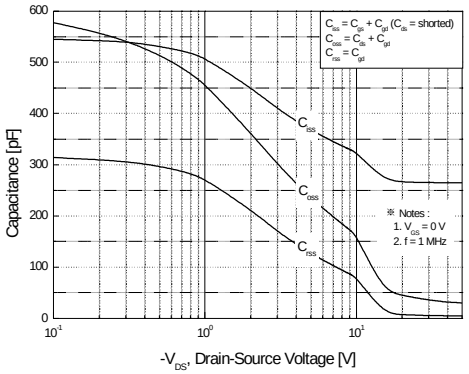

Figure 5. Capacitance Characteristics

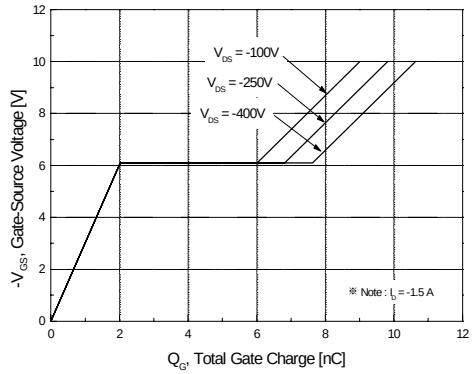

Figure 6. Gate Charge Characteristics

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Typical Characteristics (Continued)

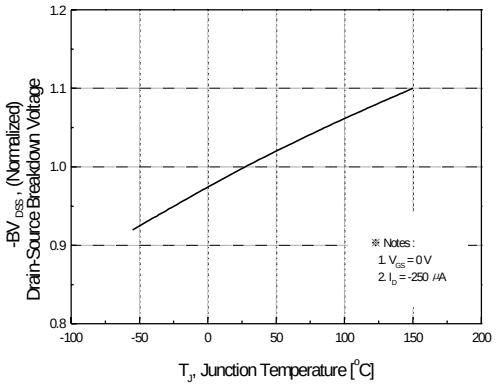

Figure 7. Breakdown Voltage Variation vs. Temperature

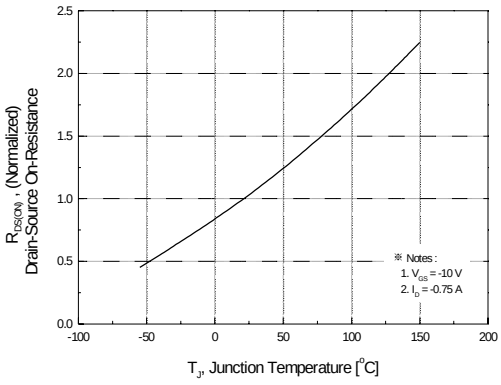

Figure 8. On-Resistance Variation vs. Temperature

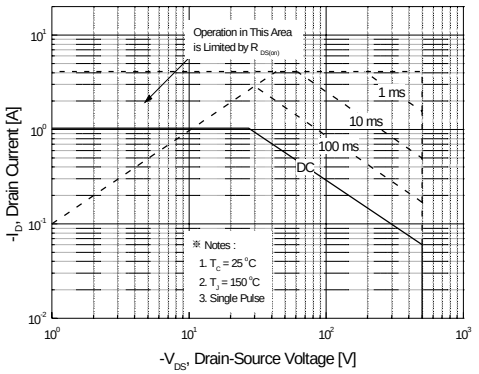

Figure 9. Maximum Safe Operating Area

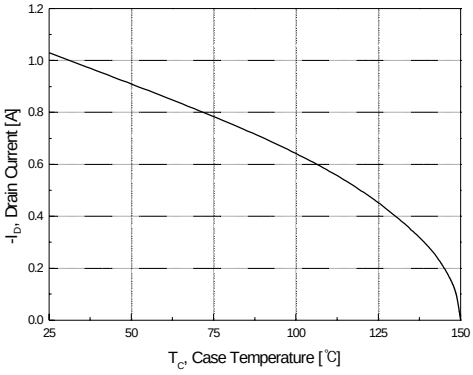

Figure 10. Maximum Drain Current vs. Case Temperature

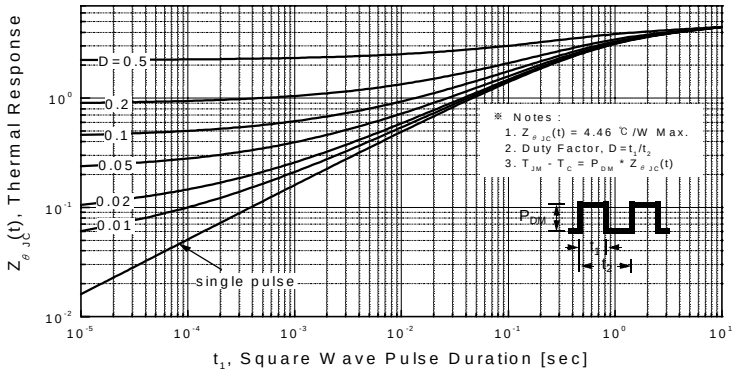

Figure 11. Transient Thermal Response Curve

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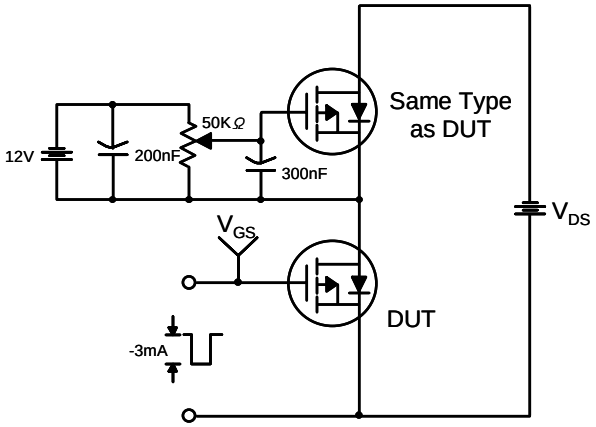
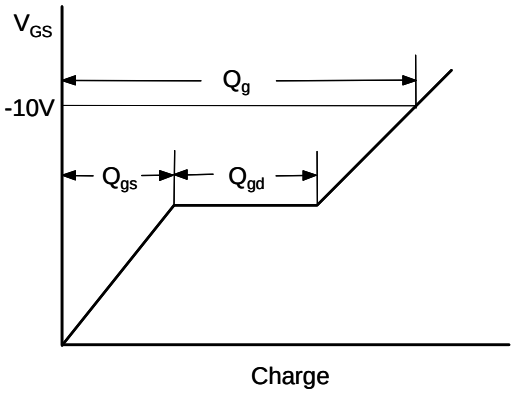
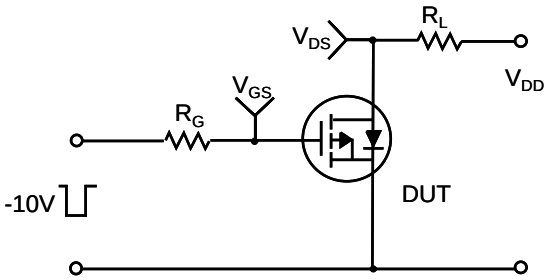
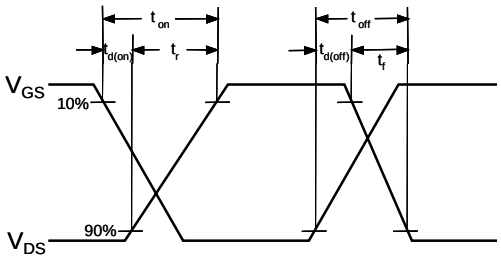
Gate Charge Test Circuit & Waveform



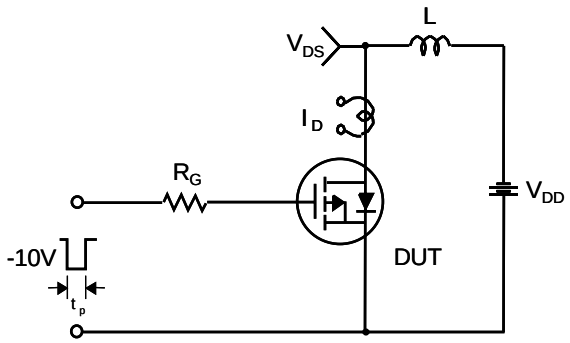


Resistive Switching Test Circuit & Waveforms

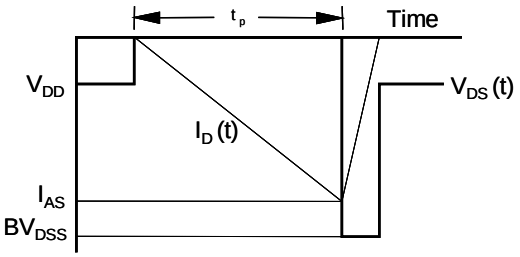




Unclamped Inductive Switching Test Circuit & Waveforms



$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



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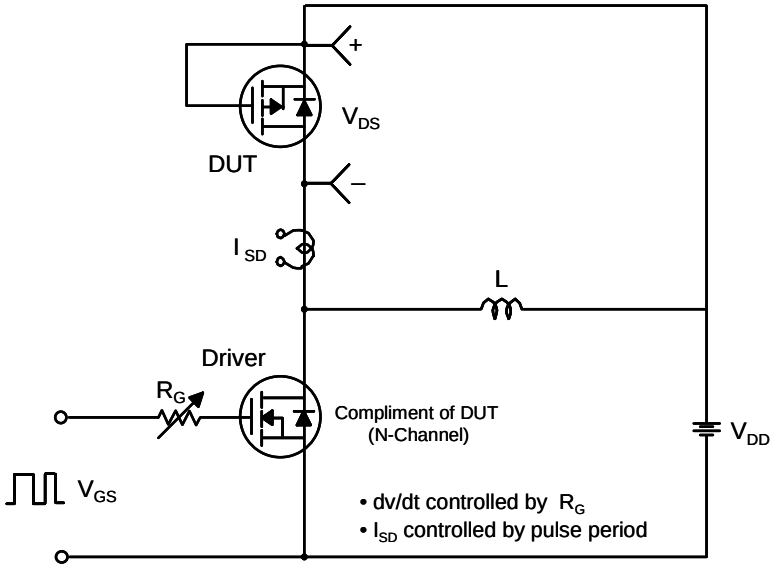
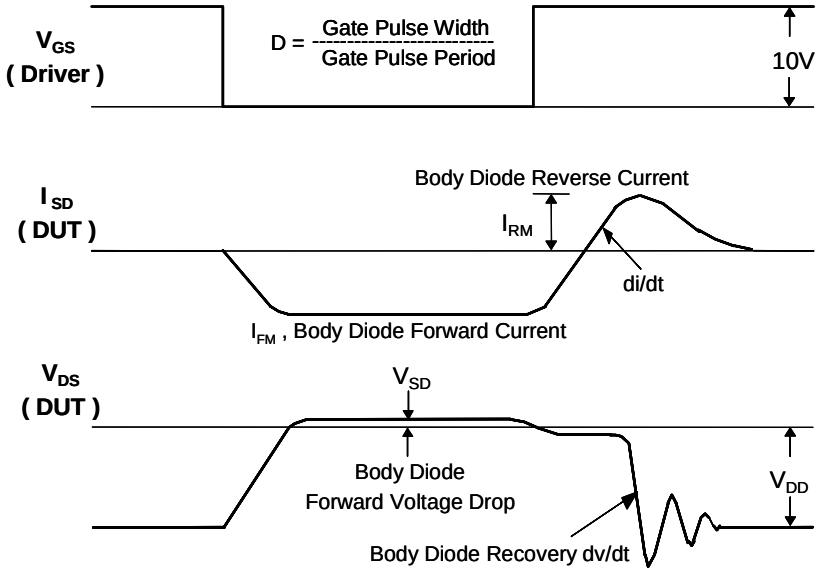
Peak Diode Recovery dv/dt Test Circuit & Waveforms





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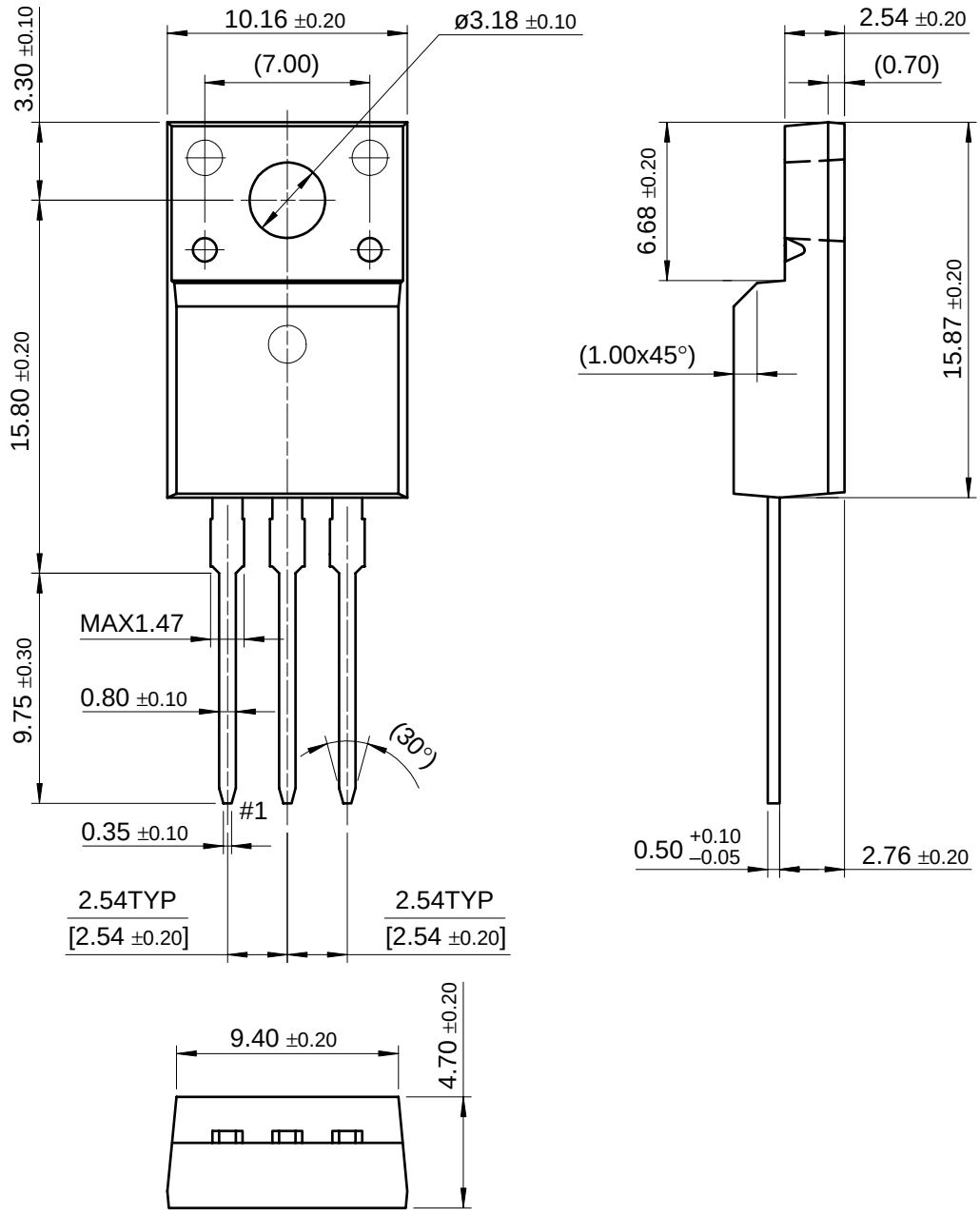
Package Dimensions

TO-220F



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